UNIVERSITY OF BIRMINGHAM | SCHOOL OF PHYSICS AND ASTRONOMY

# eRD18 - Precision Central Silicon Tracking & Vertexing for the EIC

## FY19 midterm report

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# eRD18: Proposal

To develop a detailed concept for a central silicon vertex detector for a future EIC experiment, exploring the potential advantages of fully depleted MAPS (DMAPS) technologies

**Science drivers**

Open heavy flavour decays – **high position resolution**

Precision tracking of high $Q^2$ scattered electrons – **low mass**

**WP1: Sensor Development**

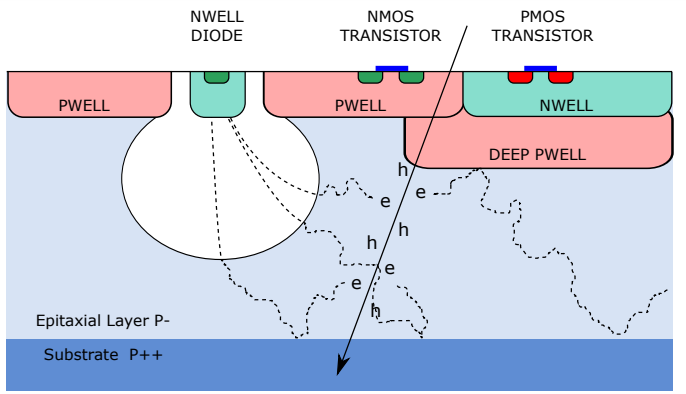
Exploit on-going R&D in Birmingham into depleted MAPS to investigate potential solutions for the EIC

**WP2: Silicon Detector Layout Investigations**

Performance requirements: numbers of layers, layout and spatial resolution of the pixel hits

# Background: State-of-the-art MAPS

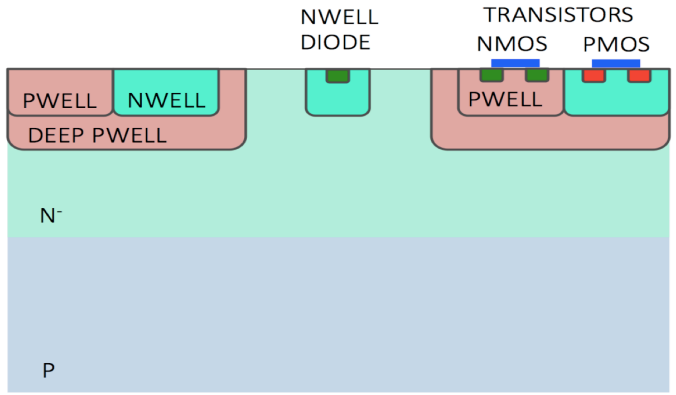
- Starting point is the ALICE ALPIDE sensor (MAPS)
  - Partially depleted; charge collection in part by drift
  - Small collection electrode = low detector capacitance




**ALPIDE sensor**

- 0.18 μm CMOS *standard* TowerJazz (TJ) process
- 28 x 28 μm$^2$ pixel pitch
- <2 μs time resolution
- Power density < 50 mW cm$^{-2}$
- 50 kHz interaction rate (Pb-Pb)
- 200 kHz interaction rate (pp)

- Future is fully depleted MAPS (DMAPS)




**CERN-TJ investigator**

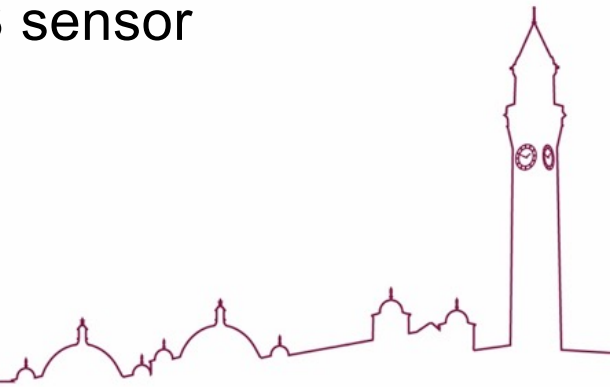
- 0.18 μm CMOS *modified* TowerJazz (TJ) process
- 20 x 20 μm$^2$ to 50 x 50 μm$^2$ pixel matrices
- Small collection electrodes
- Simple follower-based analogue readout
- Fully depleted sensor

# WP1: Sensor development

- Towards an EIC-specific DMAPS sensor
  - Aim for improved spatial resolution
    - Smaller pixels (20 x 20 $\mu m^2$ seems sufficient)
    - Low mass detector layers (< 0.3% $X/X_0$ - low power)
  - Consider readout requirements for the EIC
    - Integration time and time-stamping capability

- Technology identified: TowerJazz modified process
  - Deep planar junction allows full depletion with small collection electrode
  - Enables small pixels, low noise, and low power

- Preliminary specifications for EIC-specific DMAPS sensor
  - Based on technology investigations and survey of state-of-the-art DMAPS prototypes
  - Presented at the July meeting



# WP1: EIC-specific DMAPS specifications

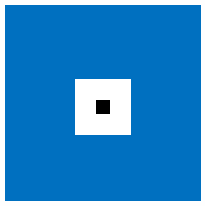
- Preliminary specifications
  - Pixel pitch ≤ 20 μm
  - Interaction rate = 500 kHz
  - Integration time ≤ 2 μs
- To minimise power
  - Small collection electrode
  - Asynchronous readout
- Fast-timing capability
  - Timestamp each bunch crossing
  - Depends on facility
    - eRHIC = 112.6 MHz
    - JLEIC = 748.5 MHz
  - 10 ns – 1 ns resolution

| | EIC DMAPS Sensor | |
|---|---|---|
| **Detector** | Vertex and Tracking | Outer Timing Layer |
| **Technology** | TJ or similar | |
| **Substrate Resistivity [kOhm cm]** | 1 | |
| **Collection Electrode** | small | |
| **Detector Capacitance [fF]** | <5 | |
| **Chip size[cm x cm]** | Full reticule | |
| **Pixel size[um x um]** | 20 x 20 | **TBD** |
| **Integration Time [ns]** | 2000 | 2000 |
| **Particle Rate [kHz/mm²]** | **TBD** | |
| **Readout Architecture** | Asynchronous | **TBD** |
| **Power [mW/cm2]** | <10 | |
| **NIEL [1MeV $n_{eq}$/cm²]** | 10^10 | |
| **TID [Mrad]** | <10 | |
| **Noise [e-]** | **TBD** | |
| **Fake Hit Rate [hits/s]** | **TBD** | |
| **Interface Requirements** | **TBD** | |
| **Timing Resolution [ns]** | N/A | <9 (eRHIC)<br><1 (MEIC) |

Updated specifications
(includes initial specs for power density)

# WP1: TJ Investigator Chips

- TJ Investigators provide test structures
  - Can be used to study the charge collection properties and detection efficiency of different pixel layouts
- Each chip has 134 matrices of 10 x 10 pixels
  - Variables are pixel pitch, electrode size and electrode spacing



Pixel: 28 x 28 $\mu m^2$
Electrode: 2 x 2 $\mu m^2$
Electrode spacing: 3 $\mu m$

Available pixel matrices

| | |
|---|---|
| 0-35: | 20 x 20 $\mu m^2$ |
| 36-57: | 22 x 22 $\mu m^2$ |
| 58-67: | 25 x 25 $\mu m^2$ |
| 68-103: | 28 x 28 $\mu m^2$ |
| 104-111: | 30 x 30 $\mu m^2$ |
| 112-123: | 40 x 40 $\mu m^2$ |
| 124-133: | 50 x 50 $\mu m^2$ |

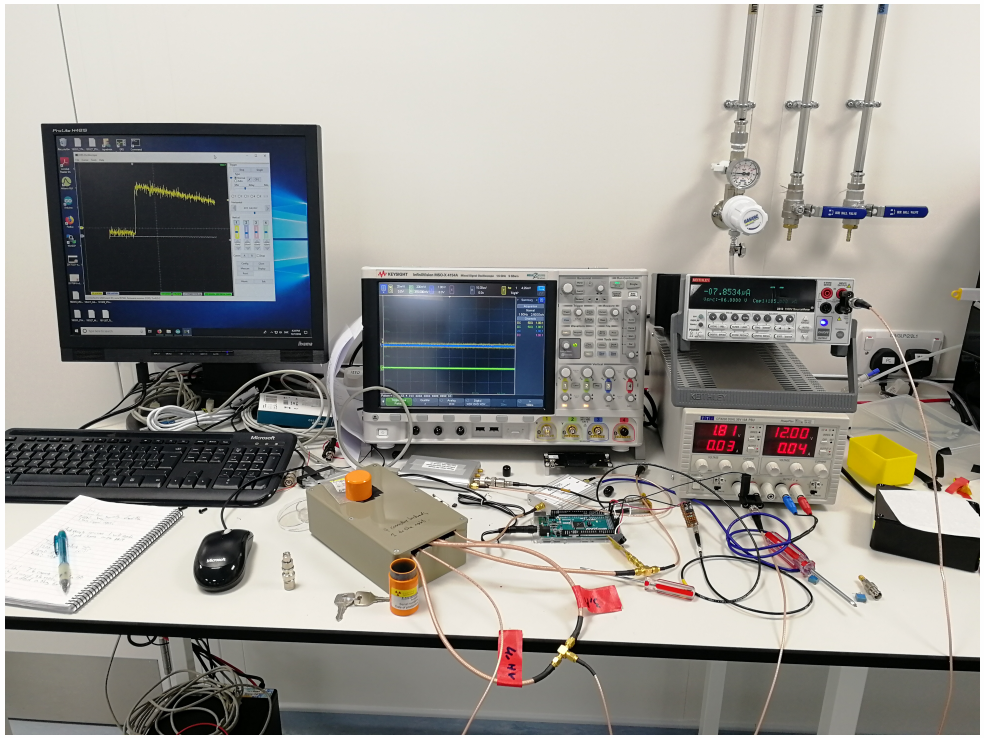
Electrode sizes
1-5 $\mu m^2$

Electrode spacing
1-5 $\mu m$ typically
(except 50 x 50 $\mu m^2$ pixels in TJ1)

- Three different versions available: TJ1, TJ1b, TJ2
- Improved charge collection in TJ1b and TJ2
  - Separate bias for p-substrate and the p-well (TJ1b and TJ2)
  - Reduced electrode spacing for 50 x 50 $\mu m^2$ pixels (TJ2)
  - Faster readout capability (TJ2)

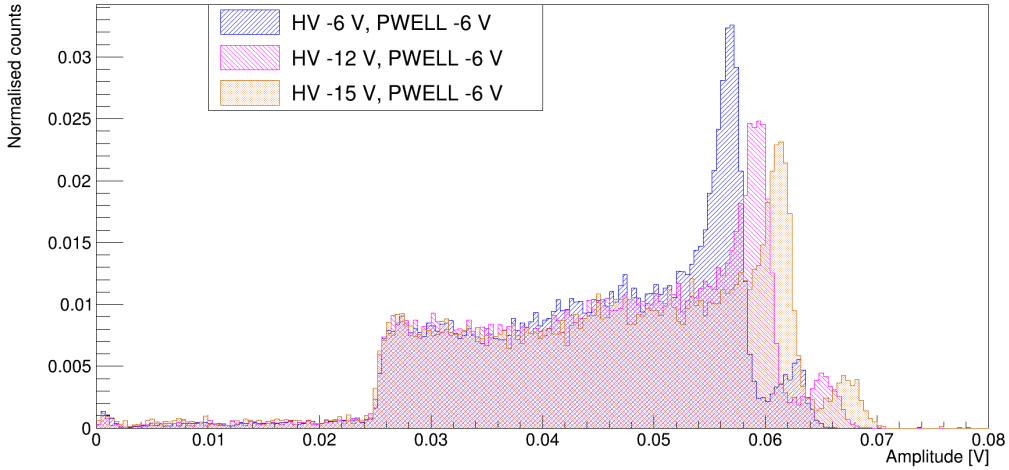
# WP1: Experimental setup and testing

- Setup development to test TJ1b and TJ2
  - The p-well and p-substrate are biased independently
  - Reset signal provided externally by an Arduino microcontroller
  - Readout done using a DRS4 USB oscilloscope
- Current tests focus on TJ1b to investigate effect of increased bias
  - $^{55}Fe$ source test on 28 x 28 $\mu m^2$ pixel



# WP1: Signal amplitude test with TJ1b

- Amplitude increases with higher bias voltage → gain change
  - Points to larger depletion with higher bias voltage
  - Leads to a change in detector capacitance




| Bias voltages | $K_\alpha$ peak [mV] | $K_\alpha$ width [mV] | $K_\beta$ peak [mV] | $K_\beta$ width [mV] |
|---|---|---|---|---|
| PWELL: -6 V, HV: -6 V | 56.72 ± 0.03 | 1.06 ± 0.02 | 62.13 ± 0.05 | 1.37 ± 0.04 |
| PWELL: -6 V, HV: -12 V | 59.05 ± 0.03 | 1.24 ± 0.03 | 65.03 ± 0.07 | 1.59 ± 0.10 |
| PWELL: -6 V, HV: -15 V | 61.11 ± 0.05 | 1.17 ± 0.04 | 67.00 ± 0.07 | 1.44 ± 0.07 |

- Further investigations ongoing to understand decrease of $K_\alpha$ peak

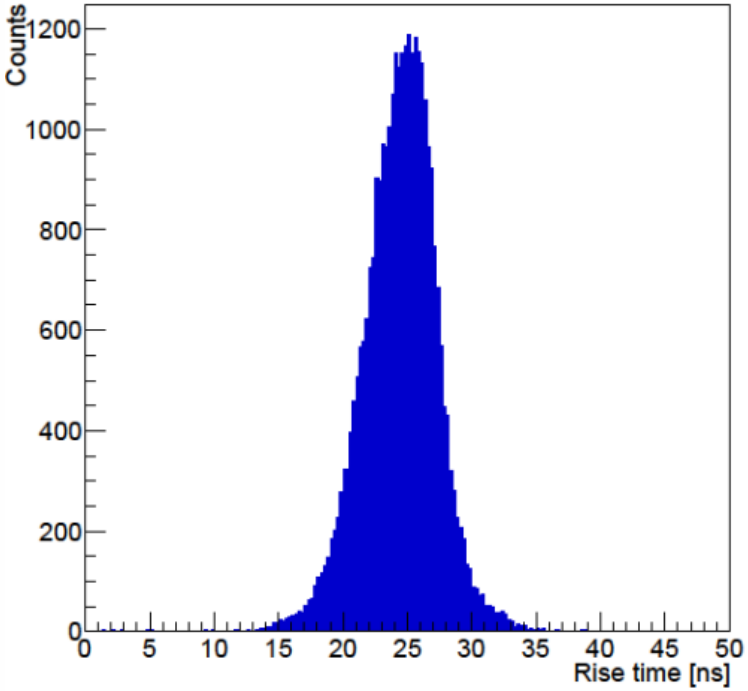
# WP1: Rise time test with TJ1b

- Find slower rise time with wider distribution for higher bias voltages
  - Points to larger depleted volume at higher bias voltage
  - More charge being collected further away from the collection electrode

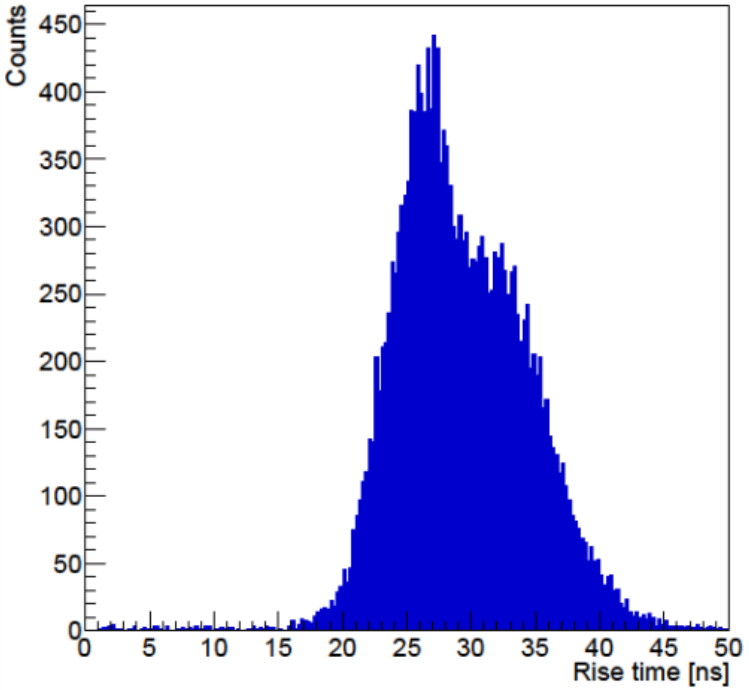
| Bias voltages | Rise time [ns] | Distribution width [ns] |
|---|---|---|
| PWELL: -6 V, HV: -6 V | 24.34 ± 0.09 | 2.87 ± 0.07 |
| PWELL: -6 V, HV: -9 V | 25.95 ± 0.09 | 2.97 ± 0.08 |
| PWELL: -6 V, HV: -12 V | 27.52 ± 0.12 | 3.94 ± 0.10 |
| PWELL: -6 V, HV: -15 V | 29.42 ± 0.17 | 4.89 ± 0.12 |

- Further investigations to verify change in depletion volume with HV
  - Study using eTCT measurements and TCAD simulations

# WP1: Rise time distributions with TJ1b




PWELL -6 V, HV -6 V




PWELL -6 V, HV -15 V

- Double-peak structure observed with higher substrate bias.
- Implies that new regions are depleted with higher bias.

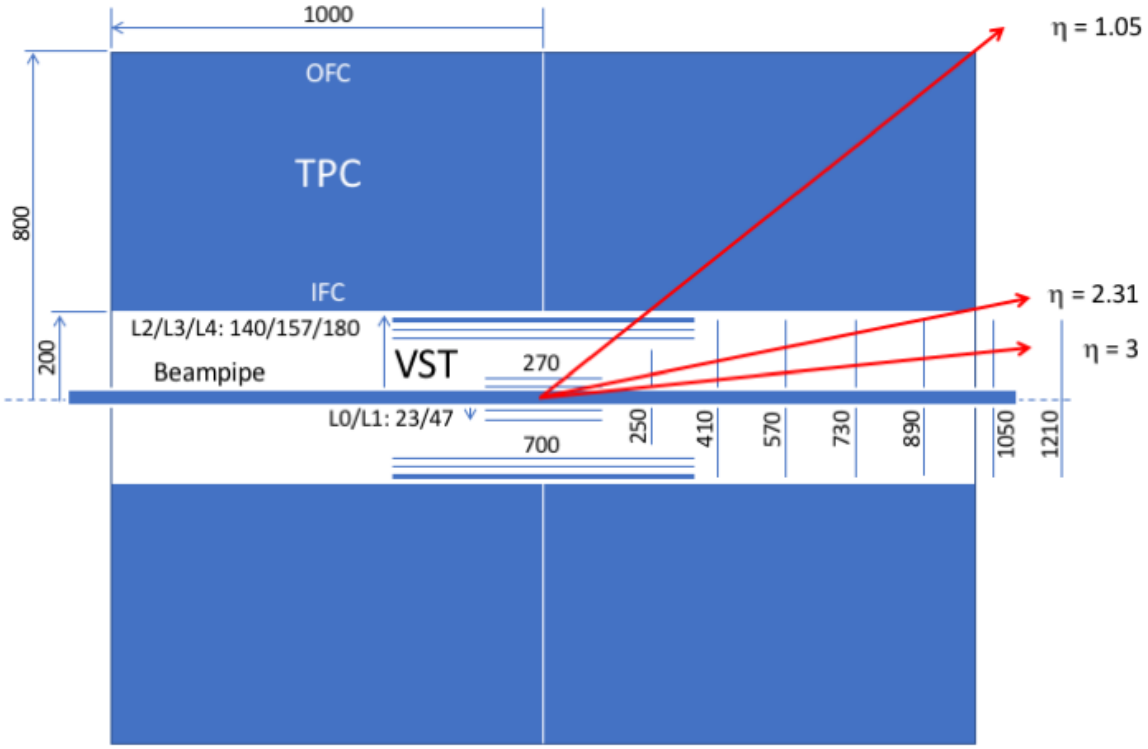
# WP1: DMAPS prototype study

- Feasibility study into the design of an EIC specific DMAPS sensor
  - Starting from the initial specifications
  - Study trade off between pixel size and power density
  - Provide realistic constraints to the detector performance studies
- Work defined with chip designer at RAL
  - First explore most demanding requirements
    - One sensor capable of both tracking/vertexing and time stamping
  - If pixel size and/or power is out of specification
    - Revert to two different chips for tracking/vertex and timing
  - The study will have two phases: pixel design, readout architecture
  - Preliminary design review held on Jan 10$^{th}$; initial specifications agreed
  - Information required: global occupancy, local occupancy, cluster size
  - Ready to start, pending contract setup at UoB

# WP1: Workplan for the next 6 months

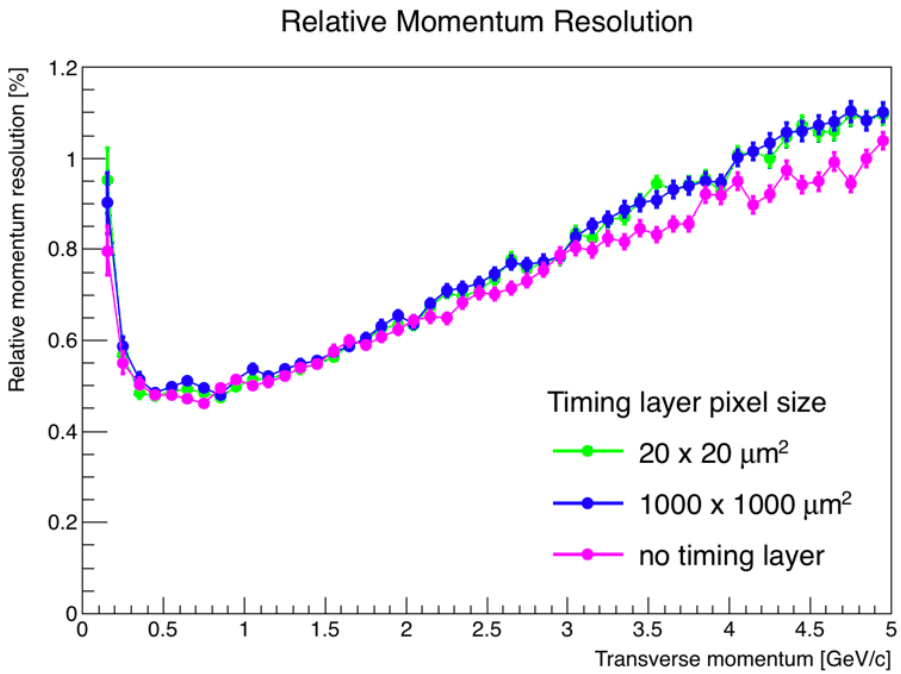
- Technology investigation
  - Complete comparison of TJ1, TJ1B, TJ2
  - In addition to source measurement, perform edge-TCT tests
  - TCAD simulations to verify results
- EIC specific DMAPS study
  - Depending on start date, complete phase 1: pixel design and possibly phase 2: readout architecture
- Possible alternative technology investigation for timing layer
  - Single-photon avalanche diode (SPAD)
  - p-n junction biased beyond breakdown voltage
  - Incident particle triggers breakdown, giving a fast signal with high gain
  - Advantages: small pixels, fast timing, high signal gain
  - Disadvantages: slow recovery after avalanche, poor radiation hardness
    - Not necessarily a problem for application at an EIC
  - Prototype from RAL available for testing

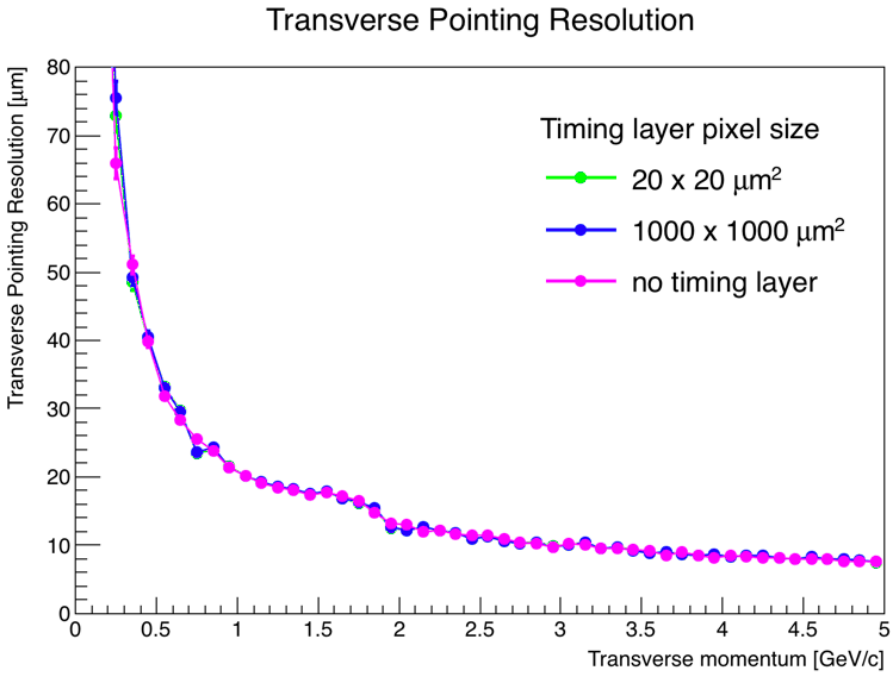
# WP2: Layout simulations




- Parameters used in the barrel simulations:
  - Pions, $0 \leq p_T \leq 5$ GeV/c, $|\eta| \leq 0.5$, B = 1.5 T
  - Timing layer 1.6% $X/X_0$, various pixel sizes
- Parameters used in the disk simulations:
  - Electrons, $\eta = 3$, $0 \leq p \leq 50$ GeV/c, B = 3 T
  - Benchmark our results with eRD16

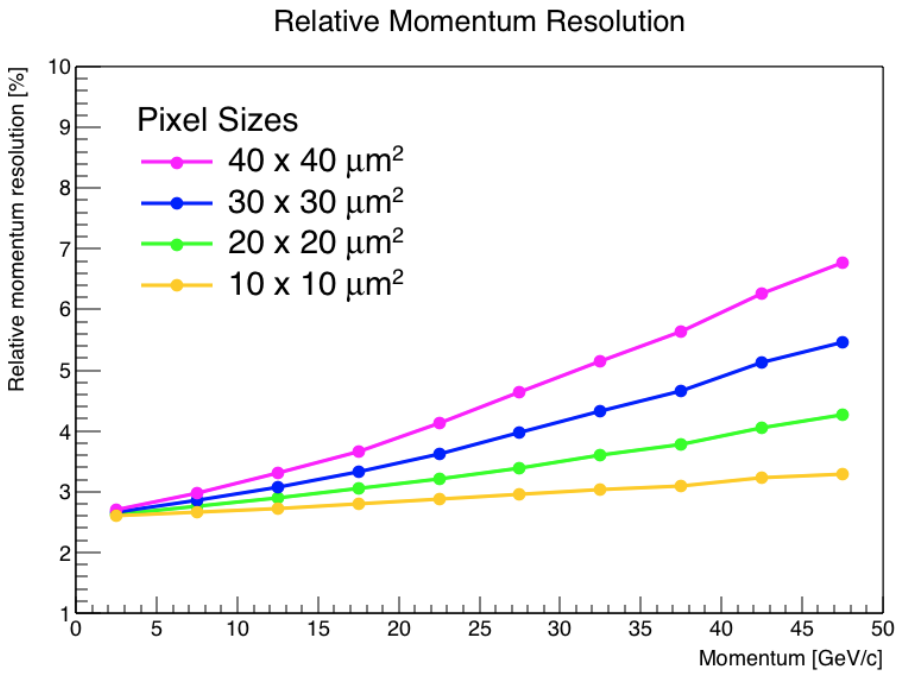
# WP2: Barrel timing layer, pixel size study

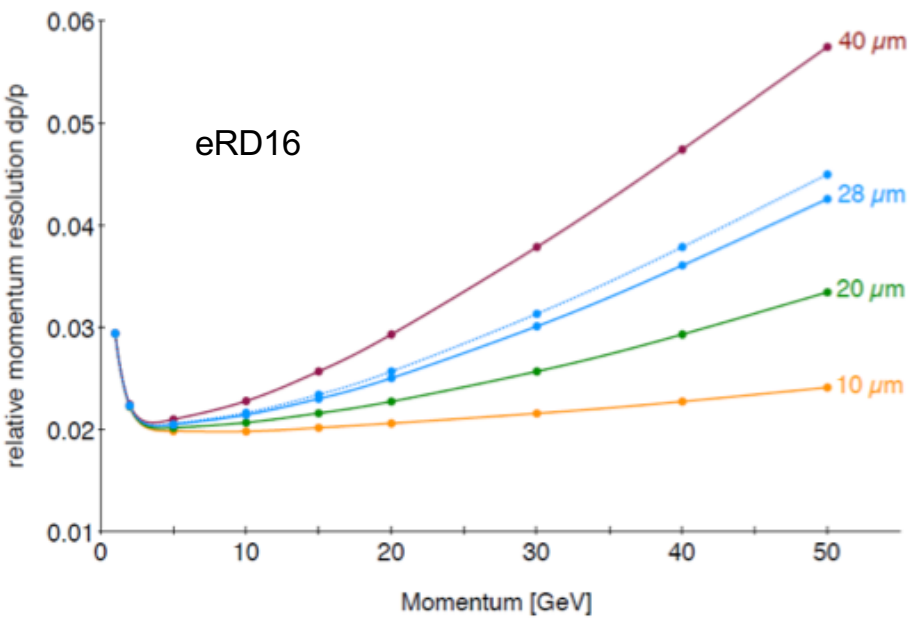



- Pions, $0 \leq p_T \leq 5$ GeV/c, $|\eta| \leq 0.5$
- 4-layer BeAST tracker, plus timing layer
- Timing layer pixel size does not affect detector performance

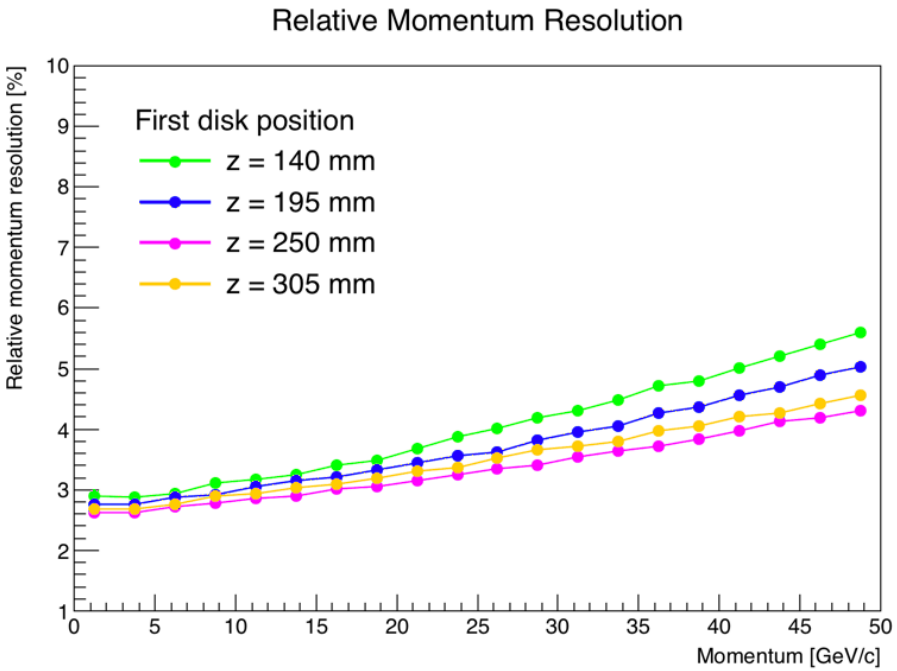
# WP2: Forward disks, comparison with eRD16

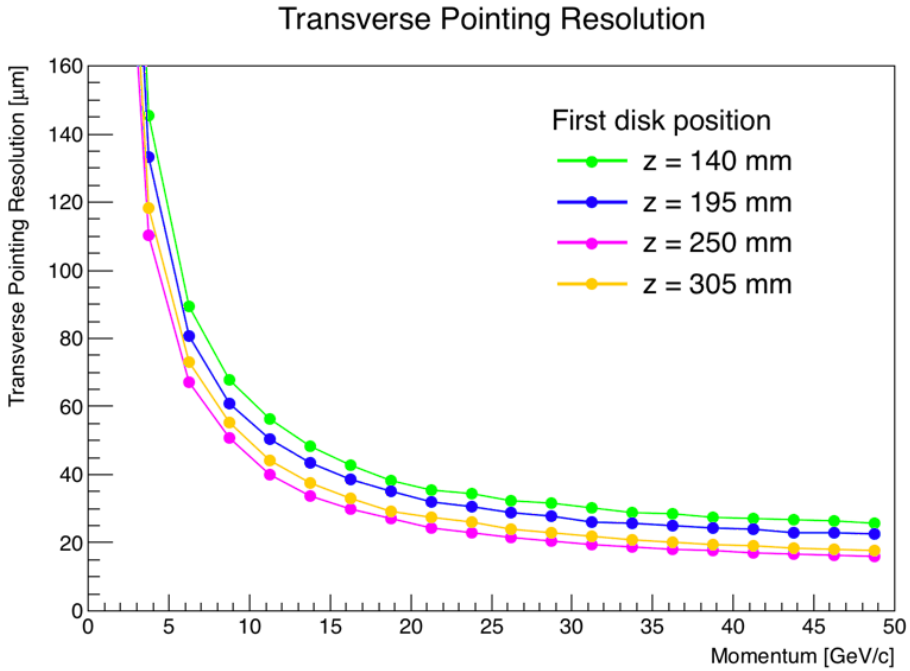



- Electrons, $\eta$ = 3, 0 ≤ p ≤ 50 GeV/c, B = 3T.
- Different pixel sizes simulated in a 7-disk configuration.
- eRD18 used EicRoot, eRD16 used a fast simulation package.
  - Upturn at low momentum due to scattering in the beampipe?
  - Possible difference in data analysis?
  - Further investigation required.

# WP2: Forward disks, innermost disk position




- Electrons, $\eta$ = 3, 0 ≤ p ≤ 50 GeV/c, B = 3T.
- Innermost disk moved, while remaining disks fixed
- Best resolution observed 250 mm from interaction point
  - At closer distances, particles at $\eta$ = 3 miss the innermost disk
  - Inner disk radius is at r = 18 mm in the simulations

# WP2: Workplan for the next 6 months

- Study tracking and vertexing in the barrel-disk interface region
  - Relative momentum resolution
  - Transverse and longitudinal pointing resolution
  - $D^0$ mass resolution
- Work with eRD16 to find the best barrel-disk configuration

# eRD18: Summary

- WP1: Sensor development
  - Finish characterisation of the modified TJ 180 nm CMOS process
  - Extend source tests with eTCT measurements
  - Explore chip design and readout options with designers at RAL
- WP2: Layout simulations
  - Explore trade offs in the interface region between barrel and disks